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Applicant:	Kao et al.	Docket No:	16405-0311
Serial No:	09/256,265	Group Art Unit	2815
Filing Date:	February 23, 1999	Examiner:	Diaz, J.

Title: **"METHOD AND APPARATUS FOR SPLIT GATE SOURCE SIDE INJECTION FLASH MEMORY CELL AND ARRAY WITH DEDICATED ERASE GATES"**

19/D
P. Walker
7-11-02

Commissioner for Patents
Washington, D.C. 20231

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JUN 25 2002
TECHNOLOGY CENTER 2800

AMENDMENT

Sir:

Responsive to the Office Action mailed March 13, 2002, please amend the above-identified application as follows:

In the Claims:

Please amend the claims as follows:

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1. (Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region defined thereon;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

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a floating gate generally disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a portion of said channel region and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a portion of said top surface of said

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